

ABSTRACT OF THE DISCLOSURE

A method for fabricating a high voltage dual gate device is disclosed which limits damage to a device isolation layer by forming a high voltage oxide film after formation of a buffer nitride film. The method includes forming high voltage n-type and p-type well regions in a high voltage device forming region of a semiconductor substrate having a low voltage device forming region and the high voltage device forming region; forming the source/drain of a high voltage NMOS transistor and the source/drain of a high voltage PMOS transistor in the well regions; forming a device isolation layer in a device isolation layer by a STI process and forming a buffer nitride film on the entire surface; forming a high voltage gate oxide film on the buffer nitride film and leaving the same intact on top of the high voltage device forming region while etching the high voltage gate oxide film and buffer nitride film disposed on the low voltage device forming region; and forming low voltage p-type and n-type well regions in the low voltage device forming region and forming a low voltage gate oxide film on the surfaces.